

Global Trigger System WBS & CORE



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WBS 1.4 Global Trigger System

1.4.1 Common Module

- 1.4.1.1 Core Design
- 1.4.1.2 Frame Firmware

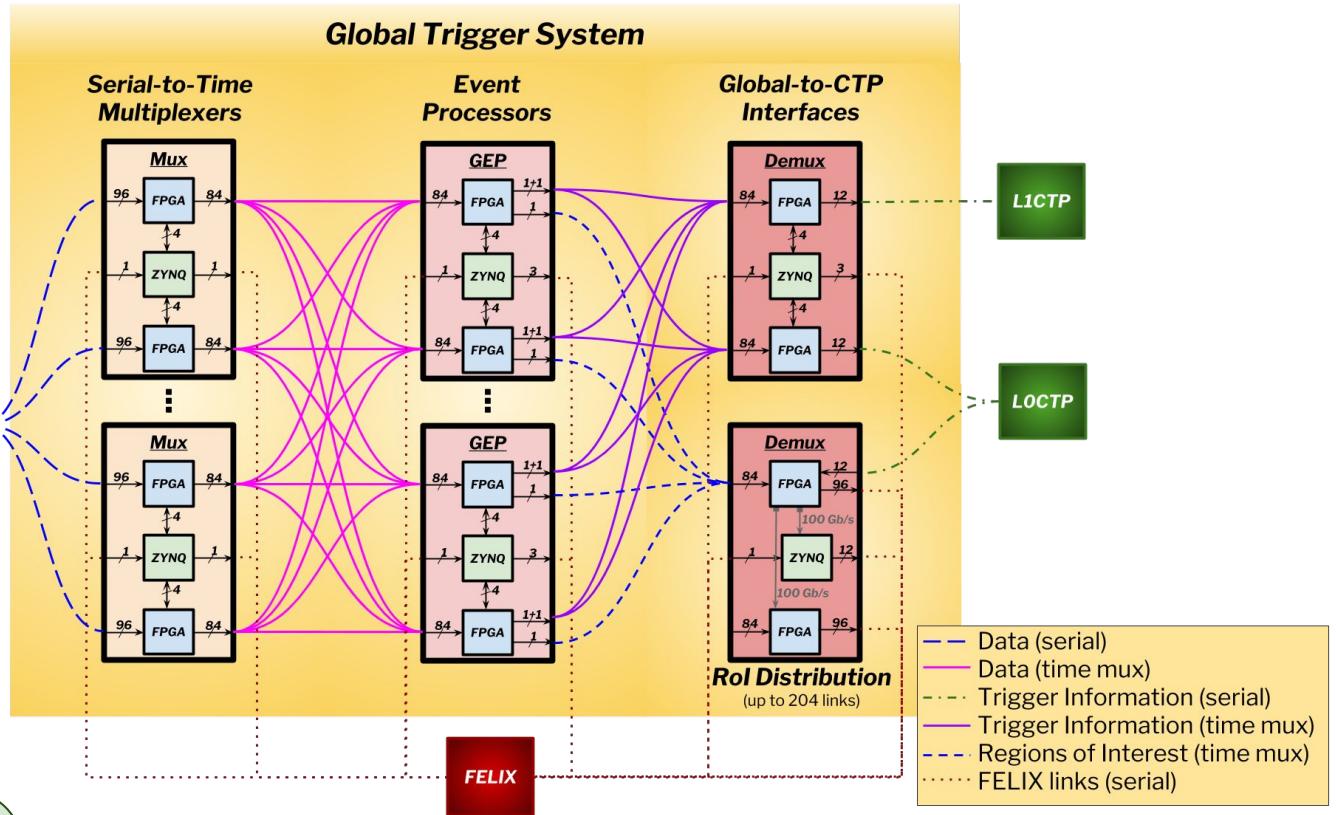
1.4.2 Interfaces

- 1.4.2.1 Multiplexer **BNL**
- 1.4.2.2 Event Processor **MSU**
- 1.4.2.3 CTP Interface
- 1.4.2.4 ROI Interface **ANL**
- 1.4.2.5 FELIX Interface **IU**

1.4.3 Trigger Signatures

- 1.4.3.1 Calorimeter
- 1.4.3.2 Tracking
- 1.4.3.3 Muon
- 1.4.3.4 EGamma
- 1.4.3.5 Tau
- 1.4.3.6 Jet
- 1.4.3.7 MissingET
- 1.4.3.8 B-Physics
- 1.4.3.9 Heavy Ion/Forward

Run 2 L1Topo had >100 algorithms proposed
We suggest organizational principle for algorithms analogous to Trigger Signature scope in HLT



1.4.4 Integration

- 1.4.4.1 Fiber Optic Plants
- 1.4.4.2 Demonstrator **ANL?**
- 1.4.4.3 ZYNQ Processor
- 1.4.4.4 Online Software
- 1.4.4.5 System Integration
- 1.4.4.6 Installation & Commissioning

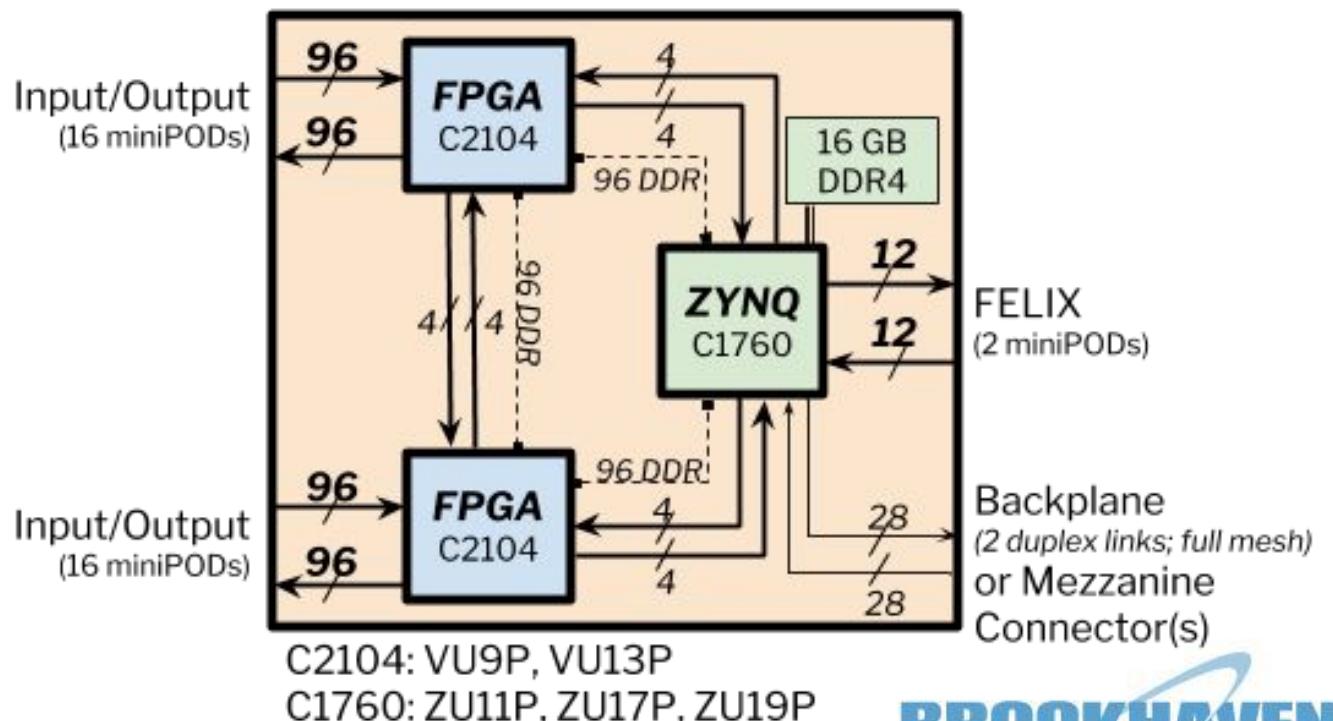
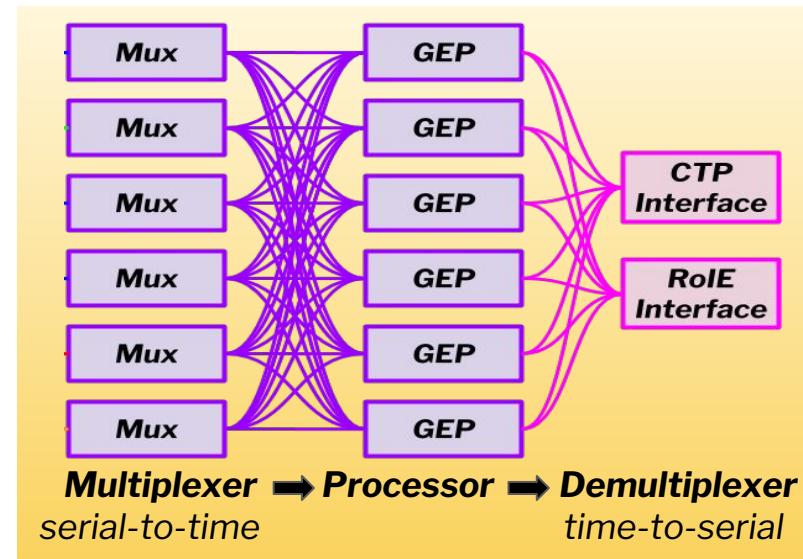
WBS 1.4.1 Common Module (GCM)

- **Common hardware platform**
 - **one ATCA module design for Global Trigger System**
 - **different functionality implemented through firmware**
 - frame firmware same for all GCM
 - minimize costs & long-term maintenance

- **Baseline architecture:**

- two Xilinx Ultrascale+ FPGA
 - **204 inputs & 204 outputs**
 - link speeds up to 25.78125 Gb/s
 - 5.2 Tb/s throughput
 - additional features:
 - one Xilinx ZYNQ Ultrascale+ MPSoC
 - inter-FPGA: 4 MGT @ 25.78125 Gb/s
 - inter-FPGA: 96 DDR → 100 Gb/s with low latency
 - 16 GB DDR4 RAM for long-latency buffering
 - 28 MGT links for full-mesh backplane or mezzanine(s)

Architecture based on today's technology.
Does not preclude post-TDR developments!



WBS 1.4.2 Interfaces

1.4.2.1 Multiplexer

- 1.4.2.1.1 Serial-to-Time Multiplexer
- 1.4.2.1.2 MUX & GEP/Unpacking & Data Org.
- 1.4.2.1.3 Protocols
- 1.4.2.1.4 Mux Integration

ZYNQ

BNL

1.4.2.2 Event Processor

- 1.4.2.2.1 Trigger Framework
- 1.4.2.2.2 GEP Integration

MSU

gMLX

1.4.2.3 CTP Interface

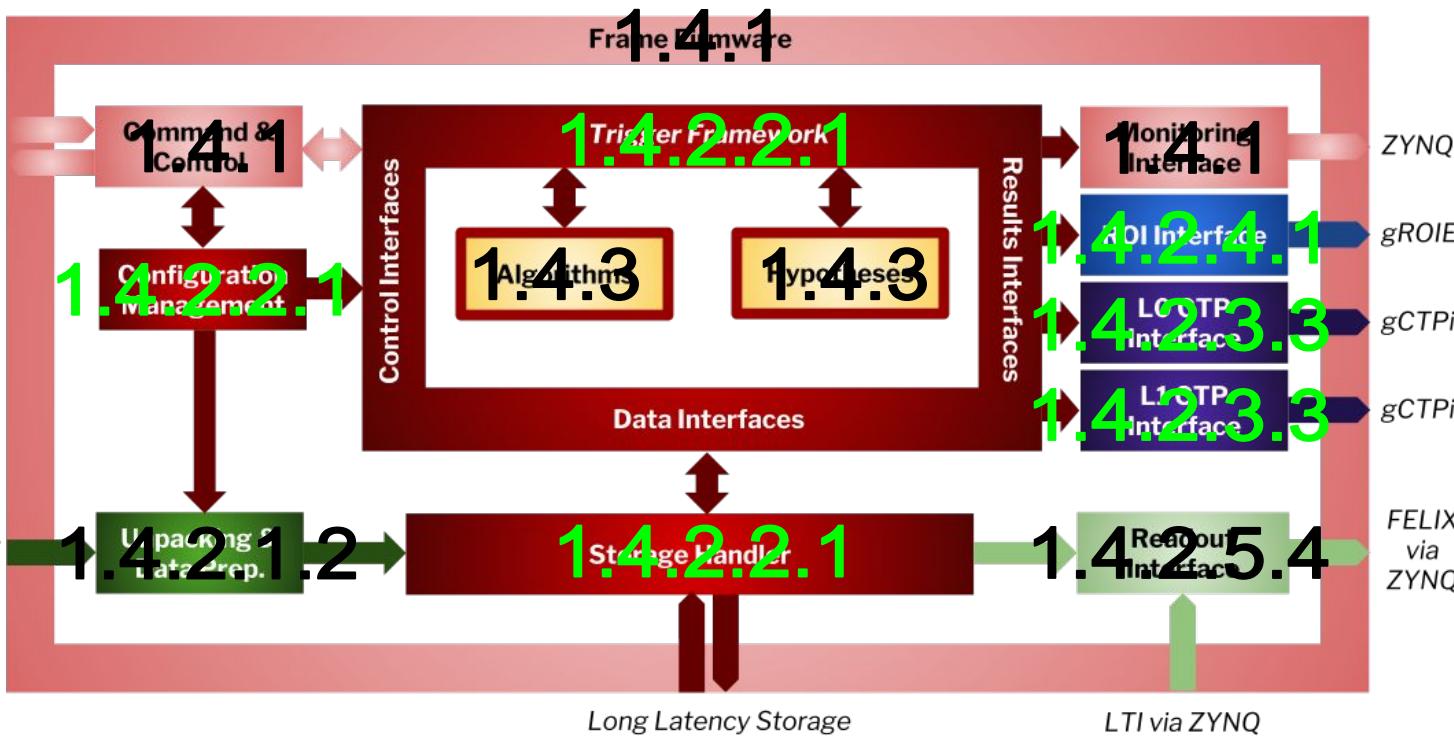
- 1.4.2.3.1 GEP/CTP Interface
- 1.4.2.3.2 Time-to-Serial Demultiplexer
- 1.4.2.3.3 gCTPi & gROIE/Trigger Items
- 1.4.2.3.4 gCTPi Integration

1.4.2.4 ROI Interface

- 1.4.2.4.1 GEP/ROI Interface
- 1.4.2.4.2 Time-to-Serial Demultiplexer
- 1.4.2.4.3 ROI-to-R3 Mapping
- 1.4.2.4.4 R3 Transmission
- 1.4.2.4.5 gROIE Integration

ANL

Event Processor Firmware (Conceptual Diagram)



1.4.2.5 FELIX Interface

- 1.4.2.5.1 Communications
- 1.4.2.5.2 Data Transmission
- 1.4.2.5.3 MUX/Readout
- 1.4.2.5.4 GEP/Readout
- 1.4.2.5.5 gCTPi/Readout
- 1.4.2.5.6 gROIE/Readout

IU

WBS 1.4.4.1 Fiber Optic Plants

- **Fiber optic patch panels:**

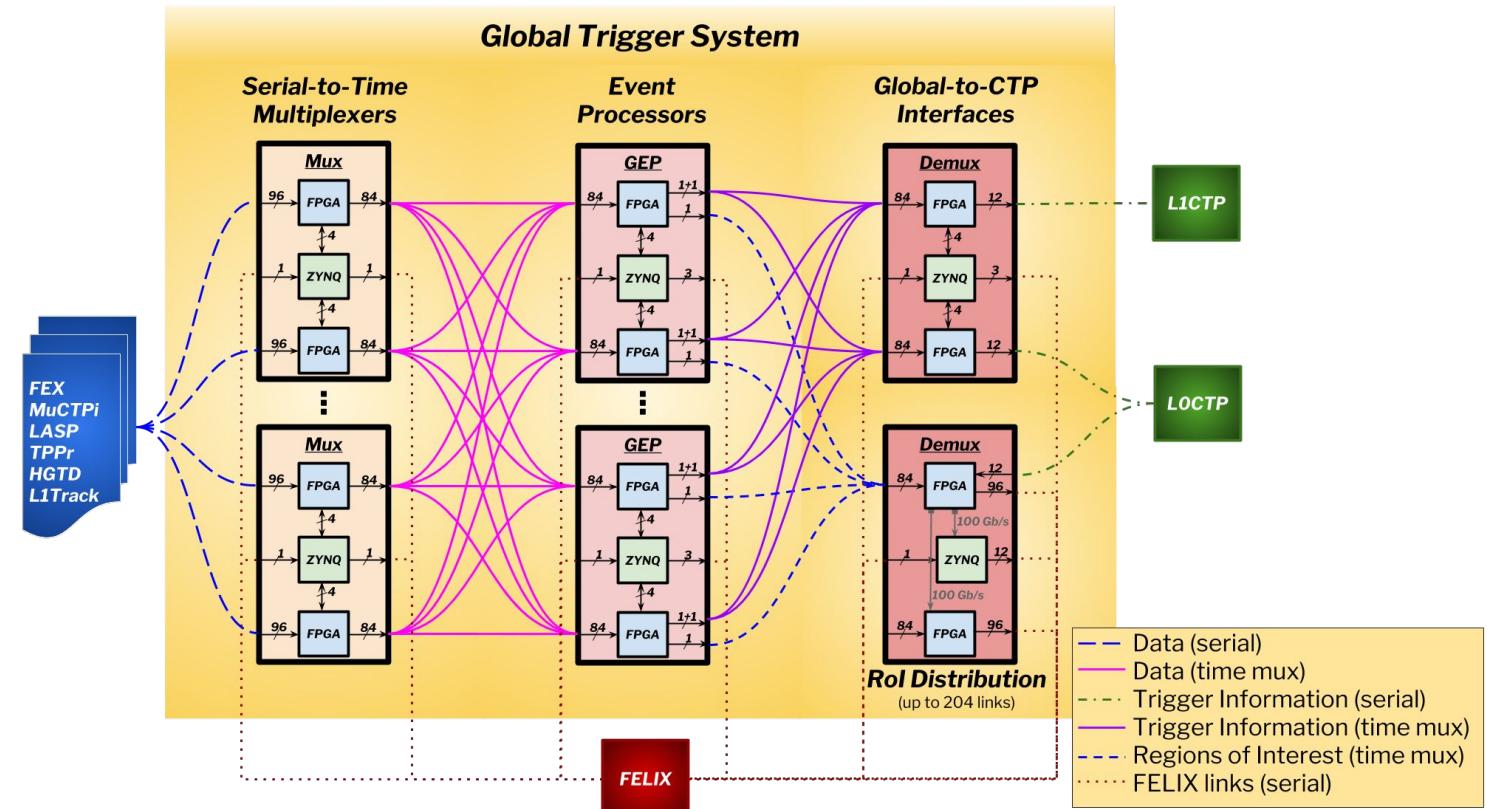
- Detectors → MUX
- MUX → GEP
- GEP → CTPi & ROIE
- ROIE → ITK/FELIX for R3 transmission
- Global ↔ FELIX

- **ATCA Rear Transition Modules**

- organize data flow through system
- needed for GEP & MUX modules

Needs proper estimate of engineering effort & CORE

Currently assume Phase-I L1Calo FOX & RTM CORE



WBS 1.4.4.2 Demonstrator

- ***Development system for Global Trigger***

- firmware development must proceed in parallel with hardware prototyping

- ***Demonstrator consists of:***

- **common** hardware platform for development
 - COTS board with appropriate FPGA preferred
- **common** firmware to support development and operate board
- **common** software for data insertion & extraction, command & control, and resource evaluation
- **common** infrastructure (power supplies, fiber optics, cabling, etc)



- ***Each Institute with a firmware deliverable needs at least one Demonstrator***

1.4.2 Interfaces

- 1.4.2.1 Multiplexer
- 1.4.2.2 Event Processor
- 1.4.2.3 CTP Interface
- 1.4.2.4 ROI Interface
- 1.4.2.5 FELIX Interface

1.4.3 Trigger Signatures

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**Demonstrator useful for
trigger algorithm development
even during Run 4**

GCM Required for Continuing Development

Prototype 2 GCM					
1 MUX	1.4.1	Common Module	1 GEP	1.4.1	Common Module
1 MUX	1.4.2.1	Multiplexer	1 GEP	1.4.2.1	Multiplexer
1 MUX	1.4.2.4	ROI Distribution	1 GEP	1.4.2.2	Event Processor
1 MUX	1.4.2.5	FELIX Interface	2 GEP	1.4.3	Trigger Signatures
1 MUX	1.4.4.3	ZYNQ Processor			
5 MUX			5 GEP		

Pre-Production GCM					
1 MUX	1.4.1	Common Module	1 GEP	1.4.1	Common Module
1 MUX	1.4.2.1	Multiplexer	1 GEP	1.4.2.1	Multiplexer
1 MUX	1.4.2.3	CTP Interface	1 GEP	1.4.2.2	Event Processor
2 MUX	1.4.2.4	ROI Distribution	4 GEP	1.4.3	Trigger Signatures
1 MUX	1.4.2.5	FELIX Interface	1 MUX	1.4.4.3	ZYNQ Processor
7 MUX			7 GEP		

Multiplexer Units Required for Operations

Data Source	Link Speed (Gb/s)	Expected Fibers	Fibers per MUX unit	MUX units
eFEX	11.2	384	96	4
jFEX	11.2	224	80	3
gFEX	11.2	16		
MuCTPi	12.8	16	16	1
LASP	25.8	1412	48	30
TPPr	11.2	352	88	4
L1Track	~10	192	96	2
HGTD	25.8	780	48	17
ROI	9.6	76?+Pixel		4
CTP	12.8	12+12	12+12	2
TOTAL			3616	67

Assume 48 Event Processors (GEP) corresponding to 24 GEP GCM

34 MUX GCM

Economies of Scale

- **Most of GCM cost is FPGAs**
 - price point depends on number of units purchased

Item	Part Number	Several	Many	Lots
PCB		\$ 1,927	\$ 1,927	\$ 1,927
Components		\$ 7,343	\$ 7,343	\$ 7,343
Zynq Ultrascale+	XCZU11EG-1FFVC1760EES9820	\$ 2,251	\$ 2,071	\$ 1,734
Virtex Ultrascale+ VU9P	XCVU9P-1FLGC2104ES9830	\$ 21,433	\$ 15,479	\$ 12,622
Virtex Ultrascale+ VU13P	XCVU13P-1FHGC2104ES9830	\$ 29,658	\$ 21,420	\$ 17,465
Mux GCM		\$ 54,387	\$ 42,298	\$ 36,248
GEP GCM		\$ 70,837	\$ 54,179	\$ 45,934

- **Centralized procurement, especially of FPGAs, is most cost-effective approach**

Proposal for Distribution of CORE Contributions

- **CORE contribution for Institute(s) responsible for WBS 1.4.1 Common Module**
 - all GCM PCB
- **One Institute, such as CERN, procures all components for all production GCM**
 - no CORE value
- **Each Institute “purchases” components for deliverables: CORE contribution**
 - Institute responsible for procurement acts as “vendor”
 - assemble boards using own company or sub-contract to Institute(s) responsible for WBS 1.4.1
 - each Institute responsible for its own testing
or
 - common assembly & testing by a (group of) Institute(s)

WBS	Deliverable	CORE
1.4.1	Common Module	\$127,000
1.4.2.1	Multiplexer	\$1,236,000
1.4.2.2	Event Processor &	
1.4.3	Trigger Signatures	\$1,188,000
1.4.2.3	CTP Interface	\$34,000
1.4.2.4	ROI Interface	\$69,000
1.4.4.1	Fiber Plant	\$240,000
	66 RTM	\$20,000
1.4.4.5	System Integration	\$93,000

U.S. CORE
Project: \$2,500,000
SUM: \$1,466,000

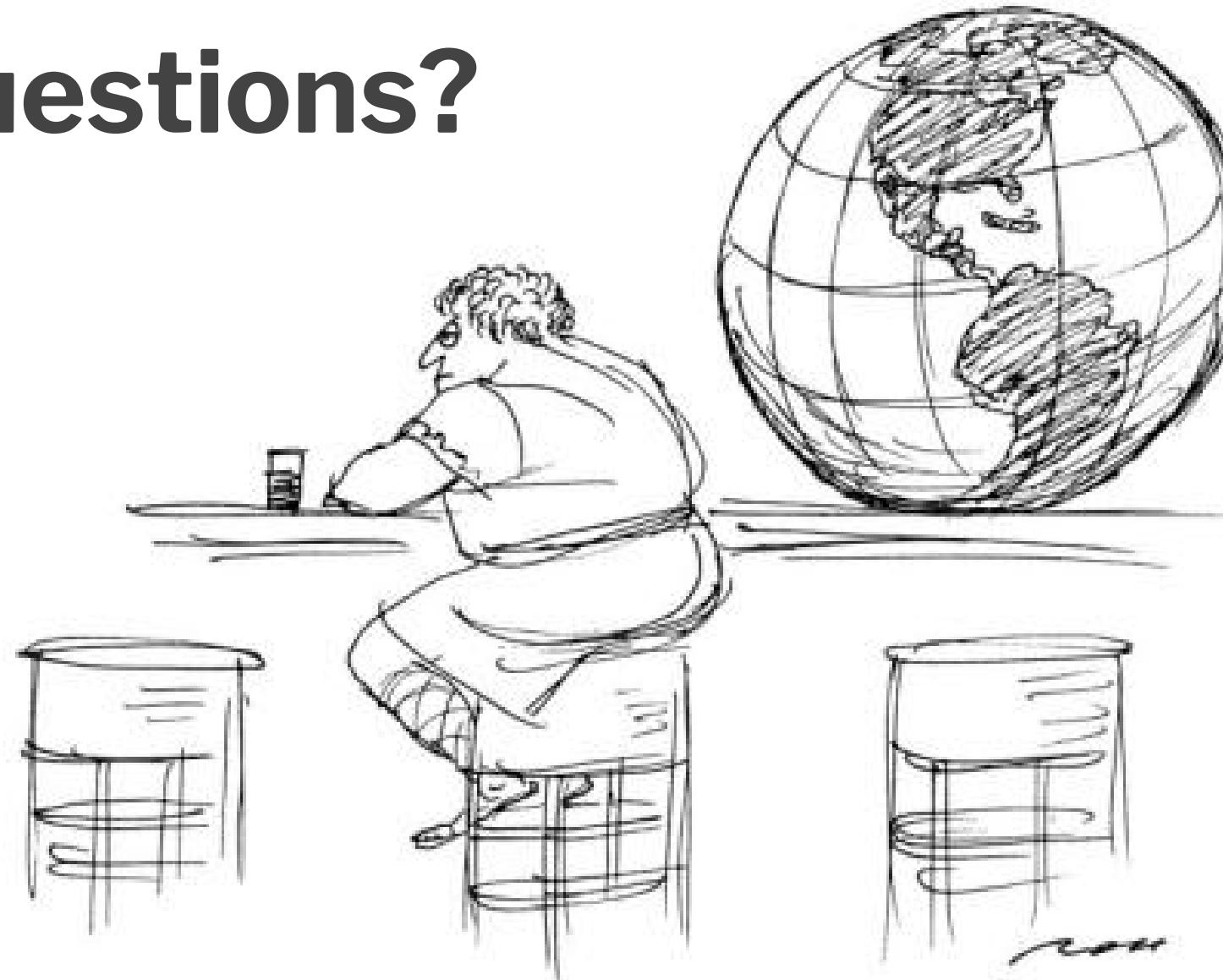
ATLAS CORE
\$3,007,000

includes 10% spares @ P1

Phase-I L1Calo FOX CORE

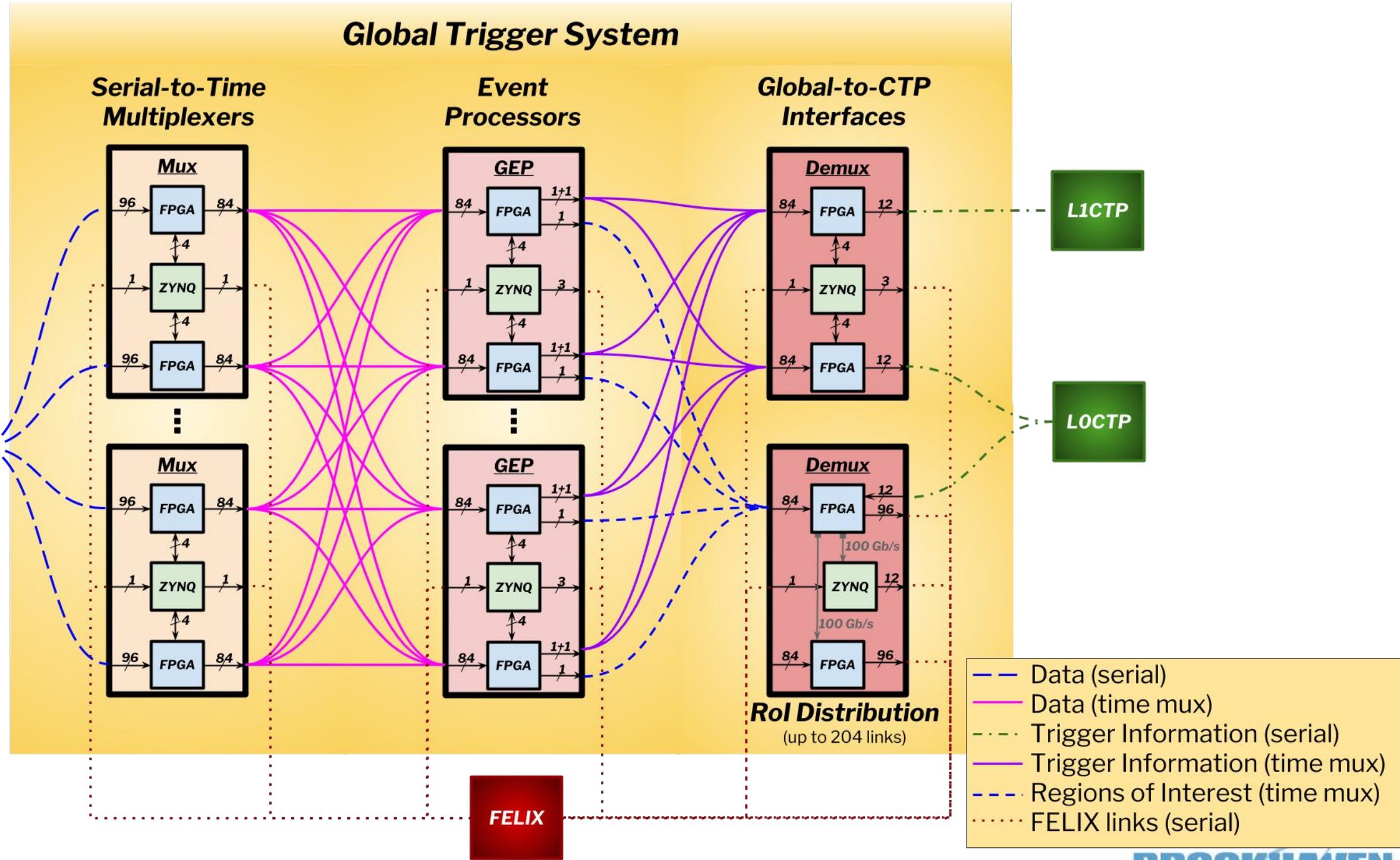
Assumes 18.5 kCHF per fully-loaded ATCA shelf

Questions?

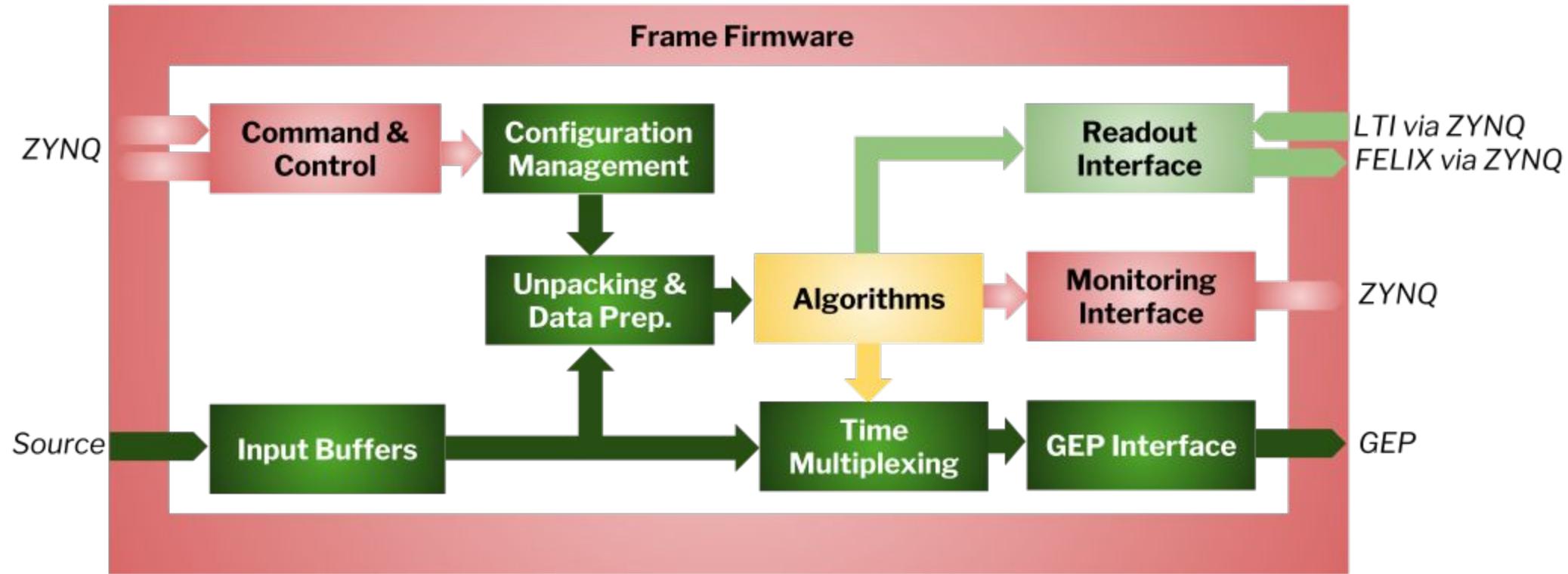


Global Trigger System

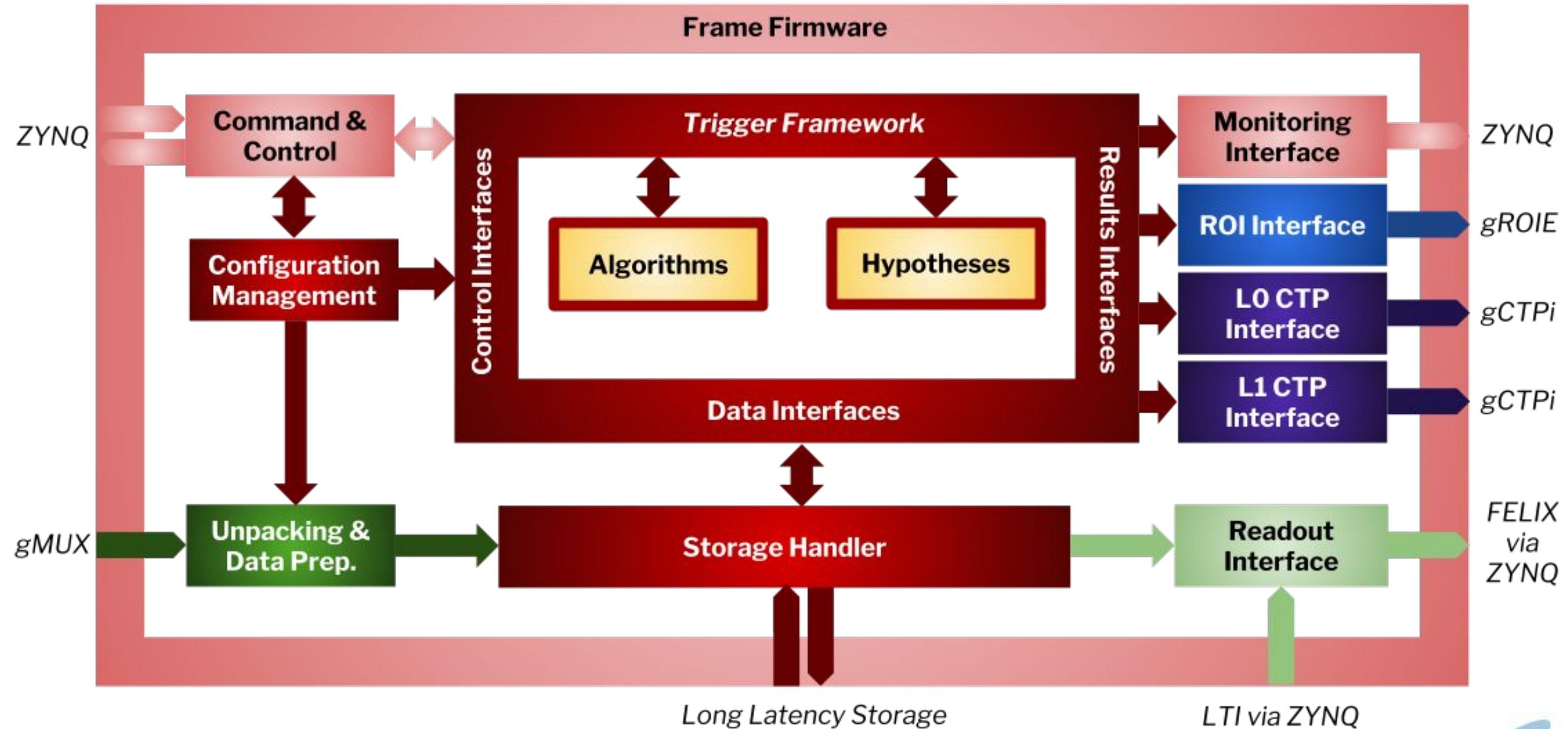
FEX
MuCTPi
LASP
TPPr
HGTD
L1Track



Multiplexer (Conceptual Diagram)



Event Processor Firmware (Conceptual Diagram)



Multiplexer → Event Processor

WBS Items

1.4.1 Common Module

1.4.2 Interfaces

1.4.2.1 Multiplexer

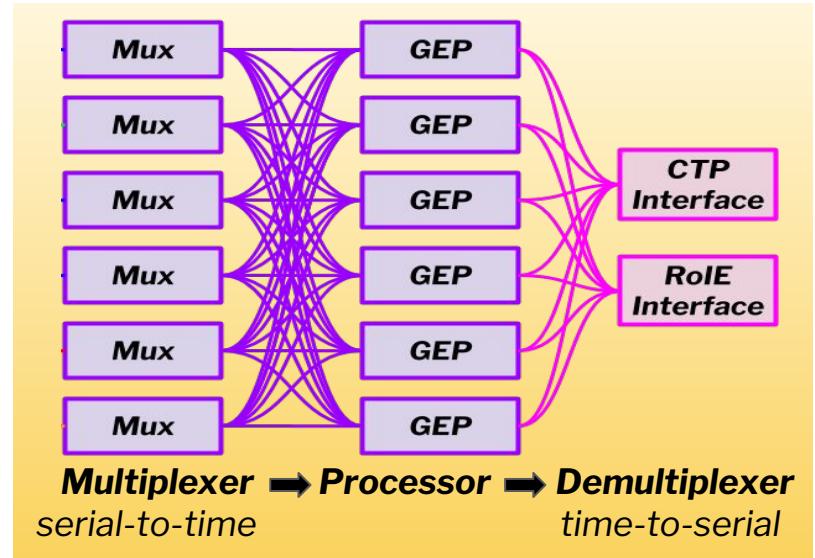
1.4.2.2 Event Processor

1.4.2.3 CTP Interface

1.4.2.4 ROI Interface

1.4.2.5 FELIX Interface

Each functional board incorporates significant contributions from multiple WBS items.



1.4.3 Trigger Signatures

